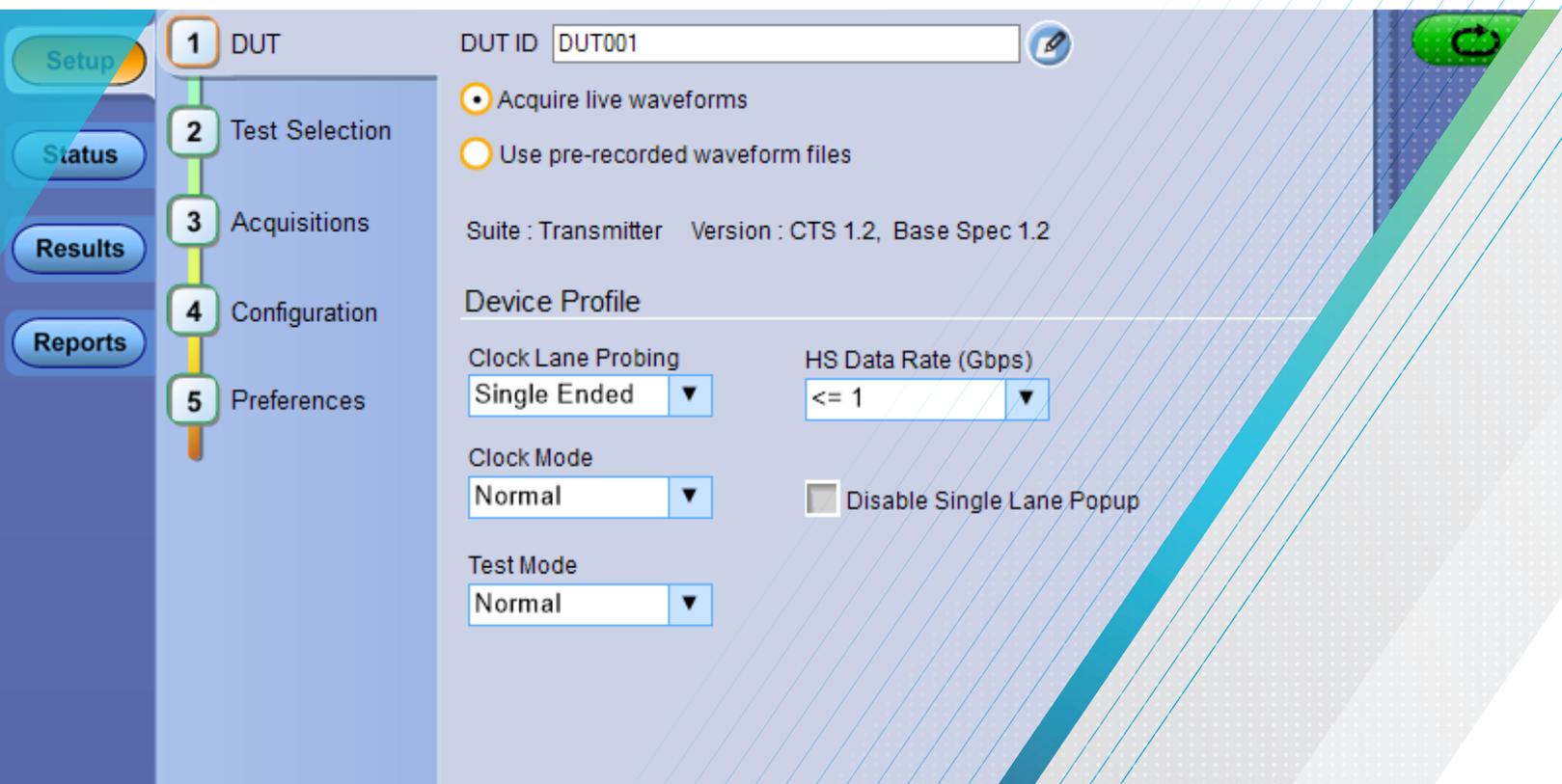


# Automated Compliance Testing of MIPI D-PHY Physical Layer

## APPLICATION NOTE



The need for high resolution displays with low power consumption is driving the adoption of high-speed serial buses, especially for mobile devices. MIPI D-PHY is a standard bus designed to transfer data between application processors, cameras, and displays. The standard is supported by the MIPI Alliance, which is a consortium of companies, predominantly from the mobile device industry. The standard is available for use by members of the alliance, and compliance testing plays an important role in insuring reliable operation of devices and interoperability among vendors. An automated system, using a reliable oscilloscope and probes, helps speed testing, improves repeatability, and simplifies reporting.

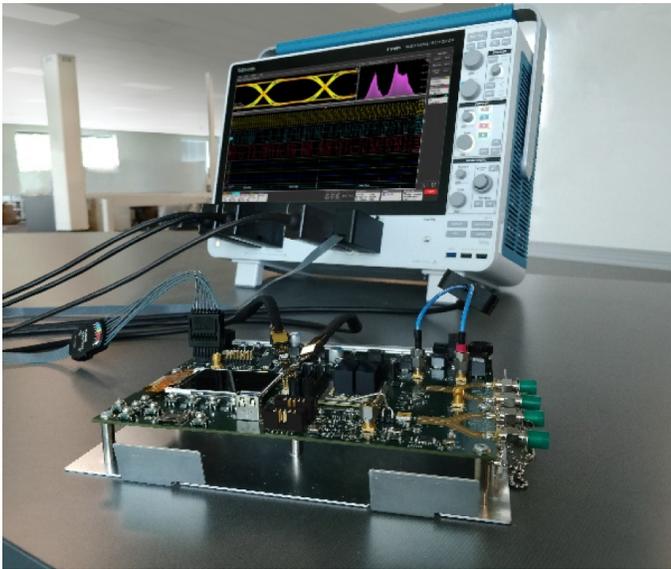
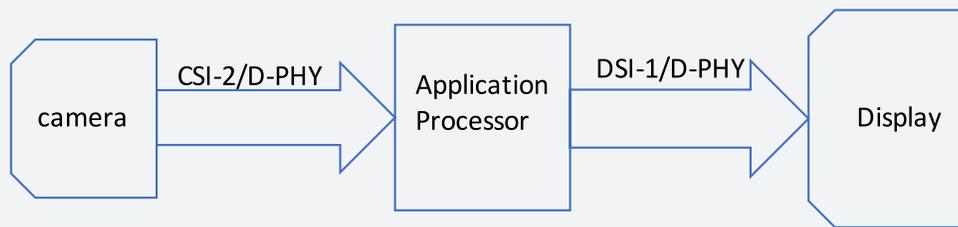


FIGURE 1. 6 Series MSO oscilloscope with high-bandwidth TriMode probes provide a solid foundation for automated compliance testing.

## Physical Layer

The physical layer of D-PHY consists of a clock and four data lanes [D0:D3] and can operate at very high speeds. The physical layer can support different protocol layers. For example, an image captured by a camera may travel to the processor over a D-PHY physical layer using CSI-2 protocol to the application processor and then to a display also over a D-PHY physical layer using DSI protocol. The CSI and DSI here refer to the protocol running over the D-PHY. The data on each of the lanes can be transferred at speeds up to 2.5 Gbps using V1.2 of the standard, or up to 4.5 Gbps, using V2.1 of the standard, to enable transfer of images with high resolution and clarity.

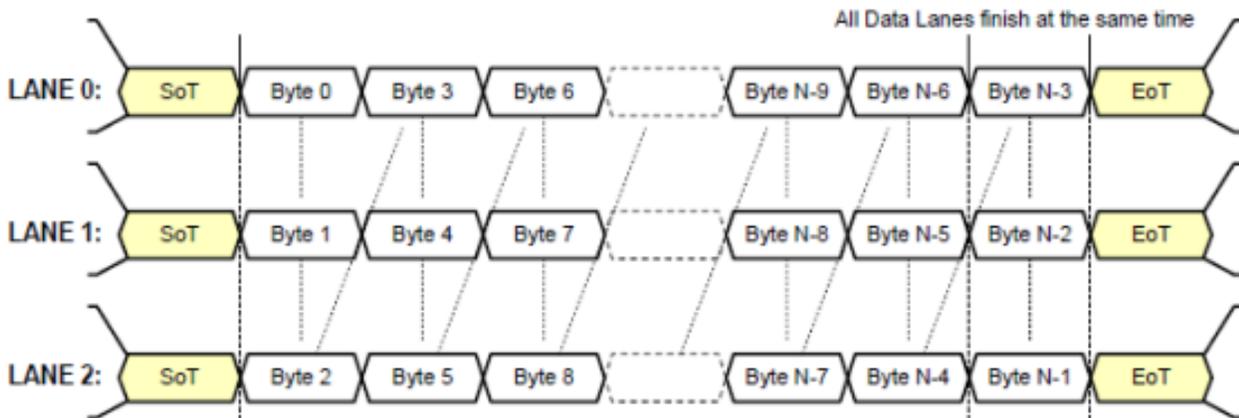
The D0 lane of the data lanes [D0:D3] is bidirectional and is used for the Bus Turn Around (BTA) function. When a host transmitter requires a response from a peripheral, it issues a request to its PHY during the last packet of the transmission. This tells the PHY layer to assert the Bus Turn-Around (BTA) command following the end-of-transmission (EoT) sequence. The rest of the lanes and clock are unidirectional. Data is striped across the lanes. For example, the first byte would transfer on D0, followed by second on D1 and so on. The fifth byte would transfer on D0. The data lane architecture is scalable from one lane to four lanes based on design requirements. Data striping on a one-clock three-lane system is explained in Figure 3. Each lane has an independent Start of Transmission (SoT) and End of Transmission (EoP). The SoT is synchronized between all the lanes. However, lanes may complete a HS transmission (EoT) before other lanes.



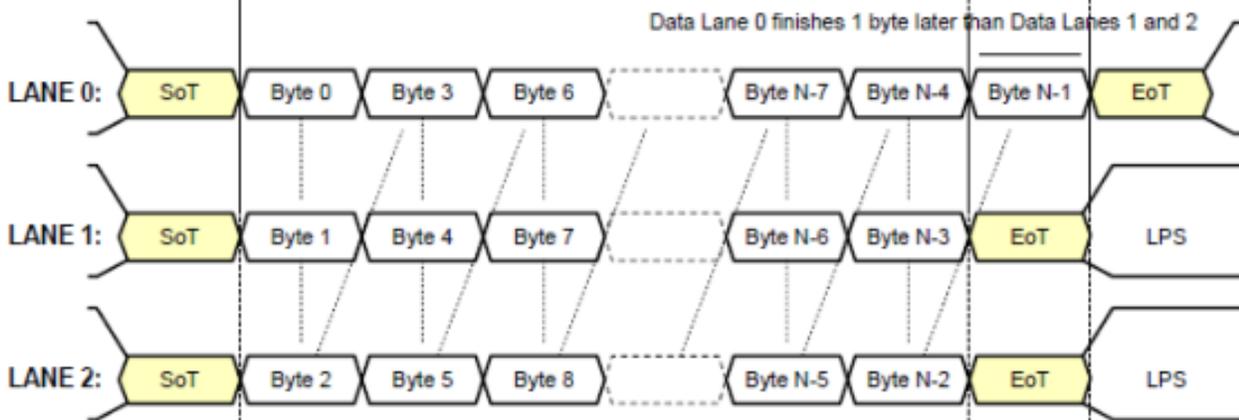
D-PHY Data flow

FIGURE 2. The D-PHY physical layer can support different protocols to optimize data transfer.

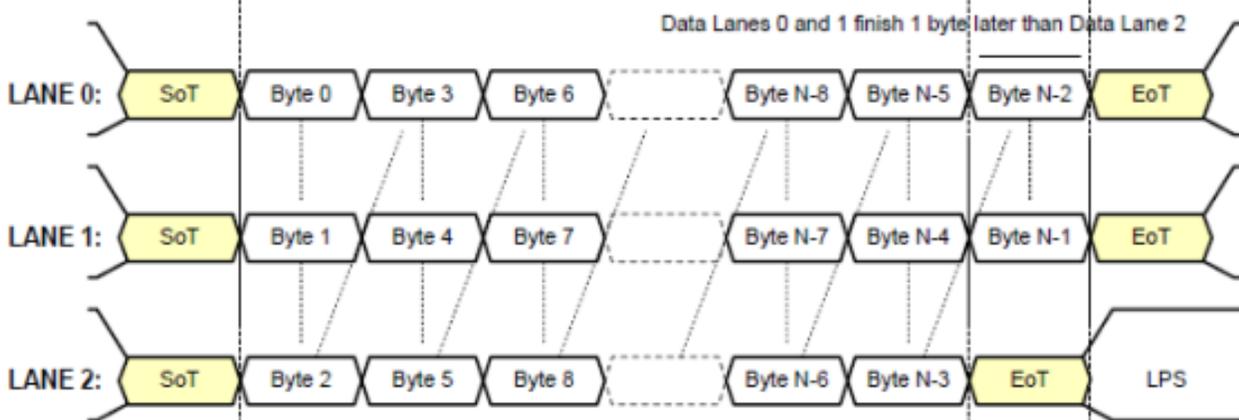
Number of Bytes, N, transmitted is an integer multiple of the number of lanes:



Number of Bytes, N, transmitted is NOT an integer multiple of the number of lanes (Example 1):



Number of Bytes, N, transmitted is NOT an integer multiple of the number of lanes (Example 2):



**KEY:**  
 LPS – Low Power State      SoT – Start of Transmission      EoT – End of Transmission

FIGURE 3. Data striping in a three-lane system. (Ref: MIPI Alliance specification for DSI v1.1)

Between the four lanes, the D-PHY 1.2 signal can have a maximum throughput of about 10 Gbps, when operating at 2.5 Gbps/lane. The physical layer signal has two modes: High Speed (HS) mode and the Low Power (LP) mode. High Speed [HS] mode is used for fast data transfers. When the system is idling Low Power [LP] mode is used to transfer control information used to conserve battery life. The HS and LP modes have different terminations and the system should be able to dynamically change termination to support both modes.

The higher the speed of the HS data, the higher the resolution that a display can support and consequently, the greater the clarity of images. To understand the relationship between data rate and resolution, we also need to look at a few more parameters.

- Pixel clock: determines the rate at which pixels are transmitted
- Refresh Rate: the number of times the screen refreshes per second
- Color depth: the number of bits used to represent a color of single pixel

The pixel clock can be derived as follows:

$$\text{Pixel Clock} = \text{Horizontal Samples} \times \text{Vertical Lines} \times \text{Refresh Rate}$$

Where Horizontal Samples and Vertical lines include the horizontal and vertical blanking intervals.

For example, a resolution of 1280x720p with refresh rate of 60 refreshes/s implies 1650x750. The difference in the horizontal samples and vertical lines is because of blanking.

In this example, the pixel clock frequency would be:

$$1650 \times 750 \times 240 = 297 \text{ MHz}$$

Let us now look at the total data rate required to support the example above. Say, for example:

$$\text{Color depth} = 24 \text{ bits}$$

$$\text{Data rate} = 297 \times 24 = 3564 \text{ Mbps}$$

$$\text{Number of lanes} = 2$$

$$\text{Then the required data rate per lane} = 1.732 \text{ Gbps/Lane.}$$

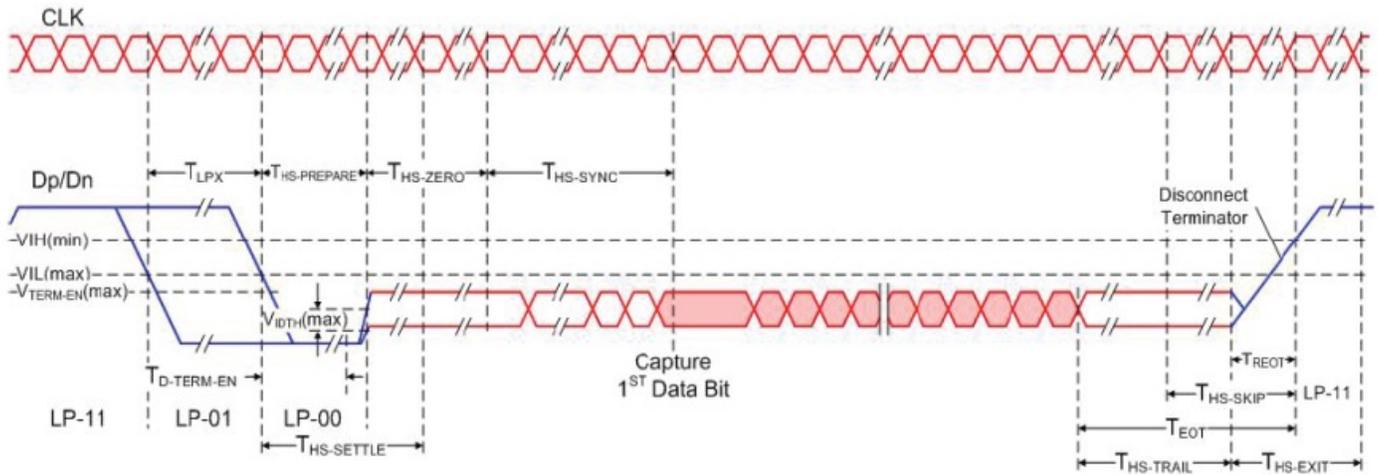


FIGURE 4. Modes and states in a D-PHY data lane in continuous clock mode. (MIPI Alliance Specification for D-PHY, Version 1.2, MIPI Alliance, Inc.)

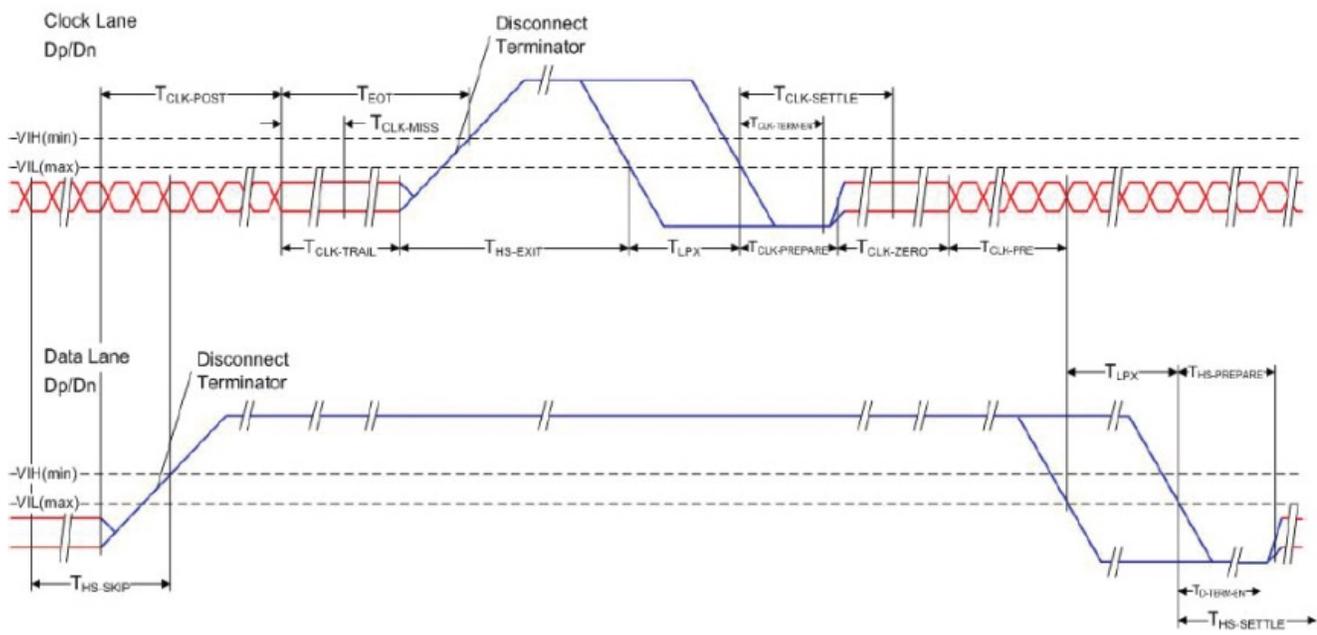


FIGURE 5. Modes and States in a D-PHY clock lane in normal clock mode. (MIPI Alliance Specification for D-PHY, Version 1.2, MIPI Alliance, Inc.)

## Electrical Signaling

Now that we know how the resolution is related to the lane speed, let us look at testing the signaling/electrical layer of D-PHY 1.2.

Data is transferred in the HS mode and when the line is idle, the transmitter switches to low power mode to conserve power. In High Speed (HS) mode, the differential voltage is 140 mV min, 200 mV nominal, 270 mV max, with the data rate extending up to 2.5 Gb/s. The HS mode consists of two possible states: Differential-0 (HS-0) and Differential-1 (HS-1).

In Low Power (LP) mode, the signaling uses two single-ended lines with 1.2 V swing, operating at a maximum data rate of 10 Mb/s. The Data Positive (Dp) line and Data Negative (Dn) line are independent of each other. Each of them can have two states 0 and 1. This results in the LP mode having four possible states: LP-00, LP-01, LP-10, and LP-11.

To accommodate the two different modes of operation, the termination at the receiver end must be dynamic. In HS mode the receiver must be terminated in 100  $\Omega$  differentially and in LP the receiver is open (un-terminated). Rise times in HS mode are different from those in LP mode.

## Probing Challenges

Dynamic termination at the receiver end complicates the testing of D-PHY signals. The probe must be capable of switching between HS and LP signals seamlessly, without loading the DUT. Most of the global timing parameters must be measured during the HS entry mode. These need to be performed as Clock alone tests, Data alone tests and Clock-to-Data tests. You also need to acquire the Clock+ (Cp), Clock- (Cn), Data+ (Dp), Data- (Dn) simultaneously, on separate channels of an oscilloscope.

Given that a 2.5 Gbps signal is the maximum speed that the D-PHY1.2 Specification supports, the minimum bandwidth required is 8 GHz. Thus, probes should have stable characteristics up to 8 GHz bandwidth, in order to be able to capture the waveforms in the transition zone of HS-LP and LP-HS.

D-PHY is becoming a popular standard in automotive display and camera applications. Testing over automotive temperature ranges can also present challenges, especially for probing.

## Test Setup

The minimum required BW for the scope and probes is 4 GHz. The recommended bandwidth for the scope and probes at the highest data rate of 2.5 Gbps is 8 GHz.

The setup includes:

- Oscilloscope
- Four (4) low-loading, single-ended probes
- TekExpress D-PHY 1.2 test automation solution
- Advanced Jitter Analysis (recommended)
- Probing/termination board

Oscilloscopes	Probes
6-Series MSO 8 GHz bandwidth	TDP7708 TriMode™ Probes and P77STFLXA x 4
MSO/DPO70000C/DX 8 GHz bandwidth or greater	P7708 TriMode Probes and P77STFLXA x 4
DPO70000SX 4 Channels, up to 33GHz BW only	P7708 TriMode Probes and P77STFLXA x 4

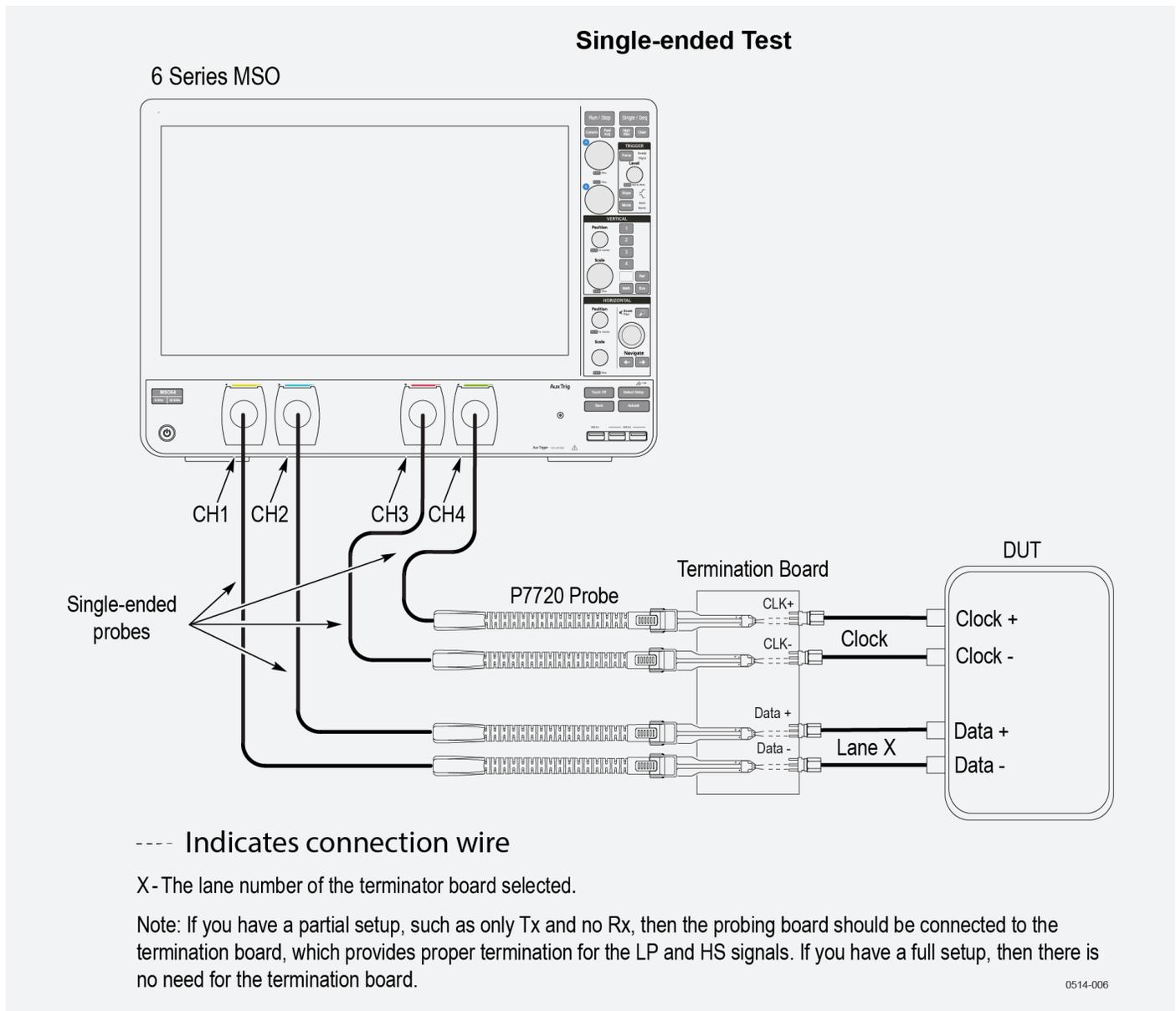


FIGURE 6. Setup for single-ended test using a 6 Series MSO.



FIGURE 7. D-PHY termination board, with TriMode probes soldered in place.

## Tests

The physical/electrical layer tests are divided into different sub groups, Group 1 to Group 6:

- Group 1 Data Lane LP-TX signaling
- Group 2 Clock Lane LP-TX signaling
- Group 3 Data Lane HS-TX signaling
- Group 4 Clock Lane HS-TX signaling
- Group 5 Clock-to-Data-Lane timing HS-TX signaling
- Group 6 INIT, ULPS, and BTA behavior

Two test signals must be provided by the DUT:

- Group 1, 2 and 6 require an Escape Mode signal from the DUT
- Group 3, 4 and 5 require a Normal Mode signal from the DUT

For example, Group 5, the data-to-clock skew test, checks the DUT performance against the permissible deviation between the data launch time and the ideal  $\frac{1}{2} UI_{ms}$ . This determines how well the data is interpreted vis-à-vis the clock. The eye diagram, as shown in Figure 8, gives a detailed view of the quality of the signal and the data-to-clock skew.

Group No.	Description	Test Signal Requirements
1	DATA LANE LP-TX SIGNALING	Escape Mode with (Ultra Low Power Sequence) ULPS Entry
2	CLOCK LANE LP-TX SIGNALING	Escape Mode with ULPS entry/exit sequences
3	DATA LANE HS-TX SIGNALING	HS Burst with both LP entry and exit
4	CLOCK LANE HS-TX SIGNALING	1. Burst Mode: HS Burst with LP entry/exit for DUTs that support burst mode 2. Continuous Mode: The LP-specific tests in this group may need to be performed separately on the leading/trailing HS entry/exit sequences that occur when the continuous clock mode is enabled/disabled
5	HS-TX CLOCK-TO-DATA LANE TIMING	HS Burst with LP entry and exit.
6	LP-TX INIT, ULPS, AND BTA	Escape mode with INIT, ULPS and BTA

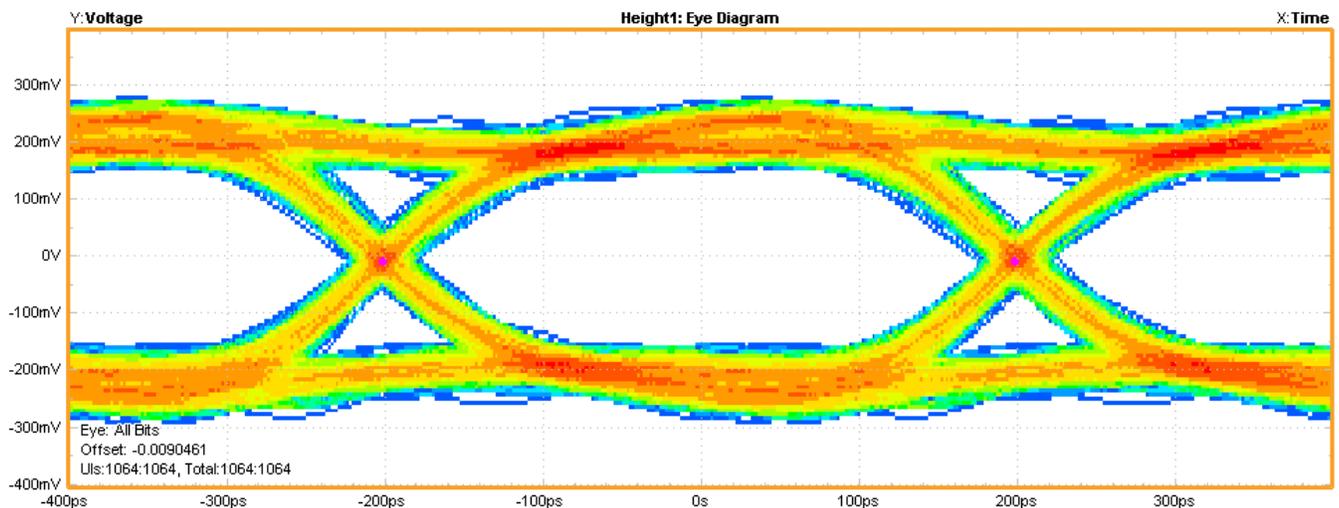


FIGURE 8. Eye diagram used in HS-TX Clock-to-Data-Lane timing test.

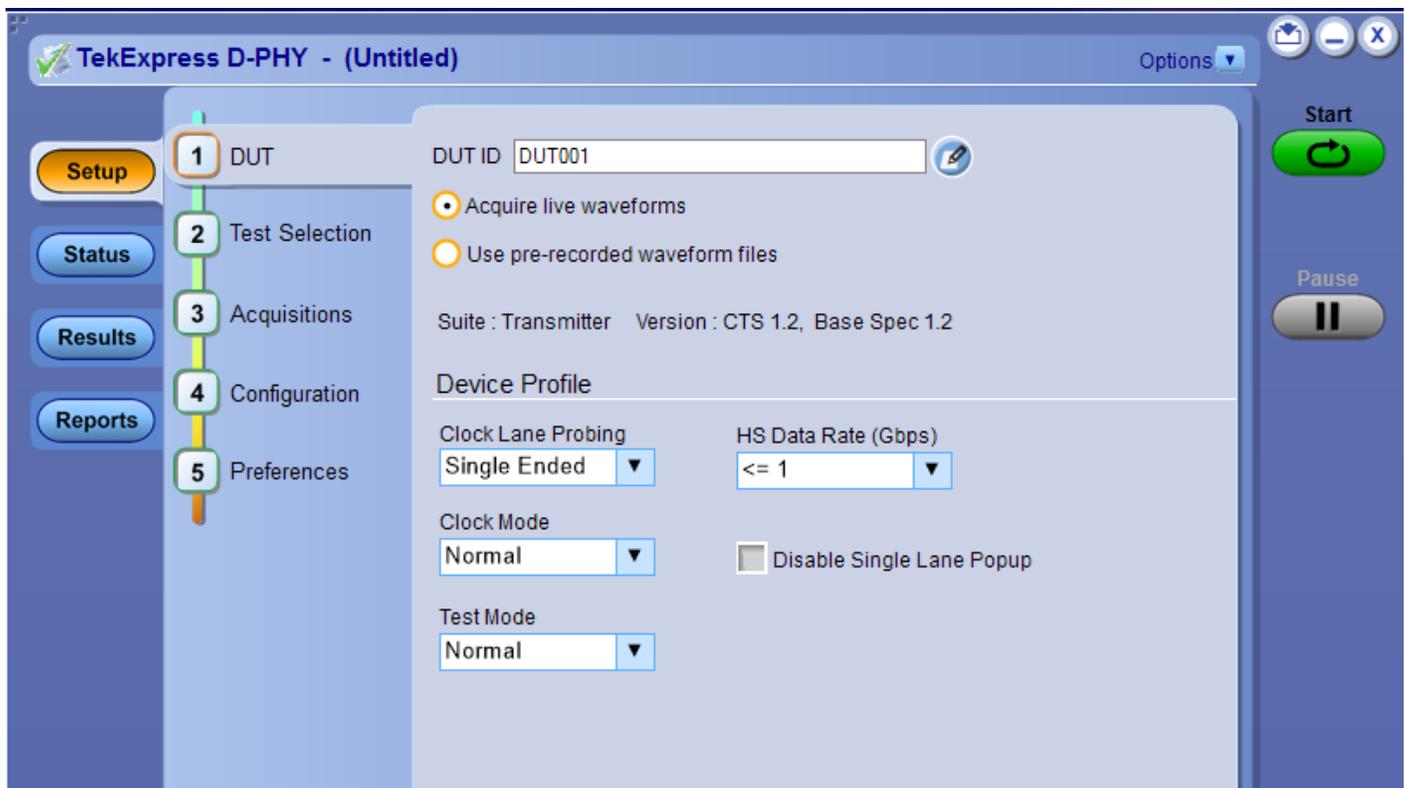


FIGURE 9. TekExpress D-PHY automation software walks you through testing – from setup to reporting.

## Automated Testing and the TekExpress Solution

The TekExpress solution integrates the fastest automated testing seamlessly with 6 Series MSO, MSO/DPO7000/DX and DPO7000SX oscilloscopes. The TekExpress software provides a graphical user interface (GUI) structured as an intuitive workflow from setting up to testing, irrespective of lane terminations. It allows you to perform compliance measurements under in-circuit operating conditions, with configurable setups, adjustable limits, and customization for DUT-specific data rates. On instruments configured with Advanced Jitter Analysis (option DJA), the TekExpress D-PHY solution plots eye diagrams for the Data-to-Clock Skew test (Test ID 1.5.4), giving visual information on the skew between data and clock.

The TekExpress automation framework is the fastest available D-PHY conformance solution, saving significant time, especially when characterizing DUT performance over various environmental conditions.

The solution can also test offline waveforms in pre-recorded mode. This allows multiple runs of data to be captured and processed later, thus saving time and effort.

Reporting supports multiple formats and customized content. Results may be grouped by test names (default), lane names or test results. Images of the first region of analysis can be included as an option. Reports not only provide Pass/Fail summary tables, but also margin details on each test in a single, consolidated report, which may be exported.

Automated compliance testing is much faster and more repeatable than manual alternatives, especially for testing the MIPI D-PHY Physical Layer. TekExpress automation software, combined with the appropriate oscilloscope and probes such as the 6 Series MSO and TDP7700, helps speed testing, improve repeatability, and simplify reporting.

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