S535 Multi-Site Wafer Acceptance Test System

Datasheet

The Keithley S535 Multi-Site Wafer Acceptance Test System is a high-power, high-speed solution for testing analog, wide bandgap (WBG), mixed-signal, and discrete devices in applications across the fab workflow. By testing two or more sites in parallel, the S535 reduces prober index time by at least 2×, therefore boosting fab productivity and lowering the cost of test.

Key Features

- Automatically perform all wafer-level DC parametric tests in multi-site parallel or serial operation. Test two or four sites in a single probe touch-down.
- Up to 64 test pins:
  - 4 sites tested in parallel, 16 pins per site
  - 2 sites tested in parallel, 32 pins per site
  - Single-site, serial operation, 64 pins
- Up to 100 W operation:
  - 100 V @ 1 A
  - 200 V @ 100 mA
- 1 fA, 10 nV resolution in a high-speed, multi-pin, fully automated test environment
- Linux-based KTE (Keithley Test Environment) system software for compatibility with legacy Keithley test systems, easy test development, and fast execution.
- Keithley S530-style Probe Card infrastructure also supports legacy S400 applications

Unlike conventional parallel test methods found on other wafer-level parametric testers, the Keithley S535's multi-site parallel test method enables testing of multiple devices on multiple sites at the same time. This eliminates any measurement dead time between test sites, therefore maximizing productivity of the tester/prober combination.

Unlike parallel test systems designed for packaged-part testing, the Keithley S535's unique combination of sub-pA and sub-µV resolution, 200V/1A/100W DC source-measure capability, and parametric wafer testing/handling software make it ideal for automated probe applications such as known good die (KGD), process control monitoring (PCM), and wafer-level reliability (WLR).

By serving multiple applications across the fab workflow with the same test platform, fabs can minimize operational and support costs while maximizing equipment utilization to lower their overall cost of ownership.

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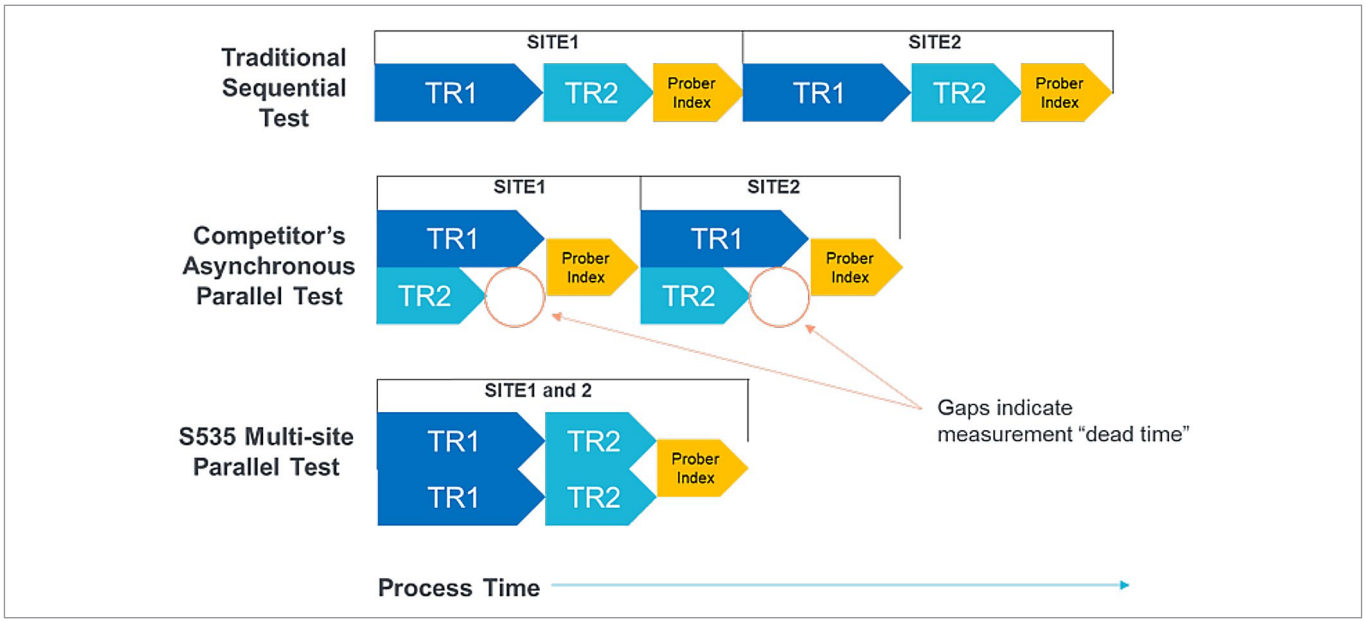
Multi-Site Parallel Test Dramatically Lowers the Cost-of-Test

The Keithley S535 can reduce test times 100% or more by testing up to four sites in parallel for each movement of the prober. This can ultimately reduce the number of probers needed to support production requirements, thus lowering overall capital investment and minimizing floorspace requirements.

Unlike conventional asynchronous parallel test schemes that test multiple devices on one site at the same time, the Keithley S535's multi-site parallel test method enables testing of multiple devices on multiple sites at the same time. Identical system resources are grouped together and dedicated for each test site. Within a given test site, each device is tested sequentially, therefore there are no restrictions on test structure design or grouping of test elements based on tester architecture.

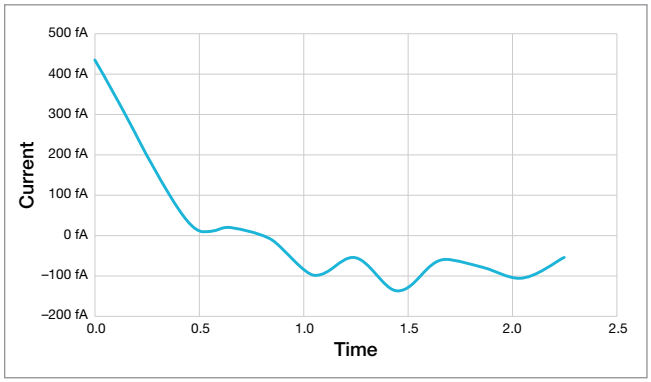
In addition, this means that there is no waiting for any tests to complete before the prober moves to the next test site, and there is no chance for measurement interaction between devices within a test site which can result in poor yields.



The S535 eliminates all measurement "dead time" between test sites, therefore maximizing productivity of the tester/prober combination and reducing overall process time.

High-Speed, Low-Level Measurement Performance

As the efficiency of today's analog and WBG semiconductor designs increase, device leakage currents and on-resistances are being driven lower and lower. The S535's low current subsystem, based on Keithley's proven SMU instrument technology, provides sub pA current measurements to support measurement of low current characteristics such as off-state leakage, gate leakage, sub-threshold leakage, and more. An optional high resolution digital multimeter (DMM) enables precise, micro-ohm level Rds-on measurements, as well as other differential and non-differential low voltage measurements such as metal sheet resistance, electrical critical dimensions, and more.



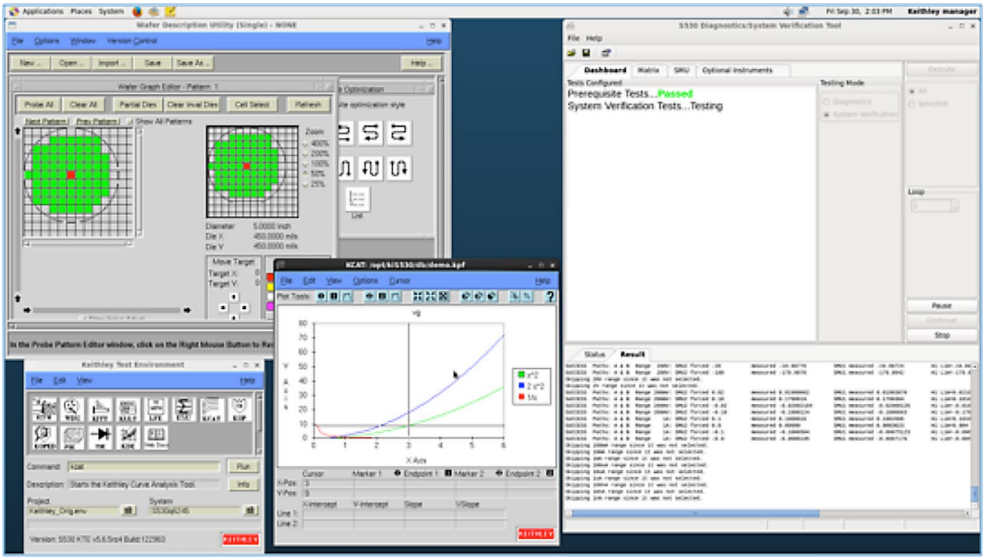
The S535 quickly settles a to sub-200 fA noise floor (12 V @ 1 PLC measurement speed).

Powerful System Software is Compatible with Existing Platforms

Keithley's S535 system features the industry-proven Keithley Test Environment (KTE) software environment for test development and execution. Our latest version, KTE v5.8, has been shown to be up to 20% faster than v5.7, thus further improving productivity and lowering the cost-of-test.

KTE incorporates decades of Keithley parametric test expertise into its feature set, and is hosted on a standard industrial PC with Linux OS. KTE software includes all the key system software operations, including:

- Wafer description
- Test macro development
- Test plan development
- Limits setting
- Wafer or cassette level testing with automatic prober control
- Test data management
- User access points
- System diagnostics



KTE software.

Measurement routines, algorithms, and test plans developed in KTE for Keithley's S400, S600, or S530 systems can be easily migrated to enable a faster production ramp-up of the S535. This re-use protects your investment and lowers overall support costs.

Keithley S400 compatibility enables a fast production ramp-up and minimizes cost-of ownership

The Keithley S535's measurement hardware, software, and mechanical interface is fully compatible with legacy S400 Series test systems. This minimizes transition costs, enables a faster production ramp-up, and lowers the cost of ownership by supporting the reuse of existing test code and probe cards. In addition, test plans developed for the S400 will run up to 2x faster on the S535, thus boosting daily productivity.

	S535	S400
Maximum Voltage	200 V	200 V
Maximum Current	2 A	2 A
Maximum Power	100 W	40 W
Current Resolution	0.1 fA	1.0 fA
Voltage Resolution	1 µV (10 nV option)	13 µV (100 nV option)
Capacitance	100 kHz – 1 MHz	100 kHz or 1 MHz
System Controller	Linux PC	Sun/Unix Workstation
Software Environment	KTE	KTE
Output Cabling	Triaxial	Quadraxial
Probe Card (up to 64 pins)	9139A	9139A

The S535 extends S400 measurement capability while maintaining backward compatibility.

S535 Condensed Specifications

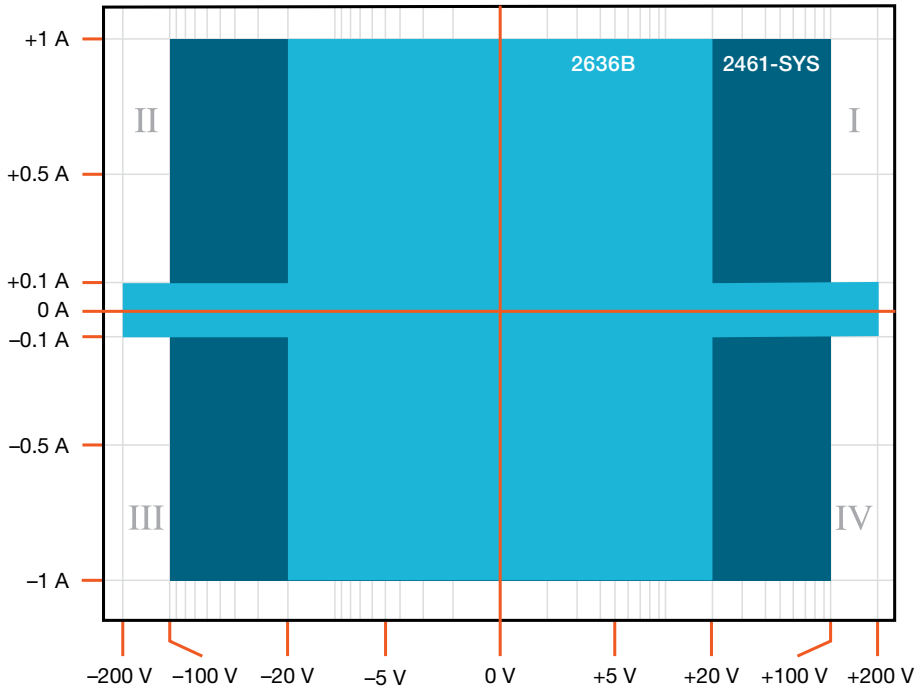
I/V Source – Measure

CURRENT[1]				
	MEASURE		SOURCE	
Range	Resolution	Accuracy (gain + offset)	Resolution	Accuracy (gain + offset)
1 A	1 µA	0.05% + 0.5 mA	50 µA	0.05% + 0.7 mA
100 mA	100 nA	0.02% + 20 µA	2 µA	0.05% + 30 µA
10 mA	10 nA	0.02% + 2.5 µA	200 nA	0.05% + 6.0 µA
1 mA	1 nA	0.02% + 200 nA	20 nA	0.05% + 300 nA
100 µA	100 pA	0.02% + 25 nA	2 nA	0.05% + 60 nA
10 µA	10 pA	0.03% + 1.5 nA	200 pA	0.05% + 5 nA
1 µA	1 pA	0.03% + 501 pA	20 pA	0.05% + 800 pA
100 nA	100 fA	0.06% + 100 pA	2 pA	0.05% + 100 pA
10 nA	10 fA	0.15% + 3.6 pA	200 fA	0.05% + 5.6 pA
1 nA	1 fA	0.15% + 880 fA	20 fA	0.05% + 2.6 pA
100 pA	0.1 fA	0.15% + 760 fA	n/a	n/a

VOLTAGE				
	MEASURE		SOURCE	
Range	Resolution	Accuracy (gain + offset)	Resolution	Accuracy (gain + offset)
200 V	1 mV	0.015% + 50 mV	5 mV	0.02% + 50 mV
100 V	100 µV	0.015% + 5 mV	2.5 mV	0.02% + 15 mV
20 V	100 µV	0.015% + 5 mV	500 µV	0.02% + 5 mV
10 V	10 µV	0.015% + 1.2 mV	250 µV	0.02% + 3 mV
7 V	1 µV	0.015% + 1.2 mV	250 µV	0.02% + 3 mV
2 V	10 µV	0.015% + 480 µV	50 µV	0.02% + 730 µV
200 mV	1 µV	0.015% + 355 µV	5 µV	0.02% + 505 µV

[1] Does not include probe card and other voltage-induced errors

SMU Operating Range



Voltage Measurement Option (Model 7510 DMM) [2]

VOLTAGE		
Range	Resolution	Accuracy (reading + range)
200 V	100 µV	22 ppm + 5 ppm
10 V	10 µV	14 ppm + 2 ppm
1 V	100 nV	15 ppm + 2 ppm
100 mV	10 nV	18 ppm + 9 ppm

[2] 7510 DMM performance is specified at instrument output terminals.

Capacitance Measurement Option (Model 4200 CVU) [3]

CAPACITANCE			
	Frequency		
Range	10 kHz	100 kHz	1 MHz
10 pF	0.50%	0.50%	1.00%
100 pF	0.50%	0.50%	1.00%
1 nF	0.50%	0.50%	4.00%
10 nF	0.50%	0.50%	5.00%
100 nF	1.00%	1.00%	5.00%

[3] Single-site mode only. Typical values.

General Specifications and Software

Cabinet Size	60.0 cm wide × 91.5 cm deep × 190.5 cm high (23.6 in. wide × 35.8 in. deep × 75 in. high)
Line Voltage	100 V, 115 V, 220 V, 240 V (50 Hz, 60 Hz)
Power Consumption	2.4 kVA for each configured power distribution unit (PDU)
Software	The Keithley Test Environment (KTE) software includes wafer description, test macro development, test plan development, limit setting, test data management, user access points, and system diagnostics
Probe Cards	Keithley, Celadon, or user-supplied
EMC	Complies with the European Union EMC Directive
Safety	Complies with the European Union Low Voltage Directive
Certifications	SEMI S2, S8, and S14
Warranty	One year
Support Services	Contracts available for probe station integration, calibration, repair, test plan migration, and correlation studies
Specification Conditions	23°C ± 5°C, 1 year calibration cycle for individual instruments, 1 power line cycle (PLC), 4-wire (Kelvin) configuration. Subject to change without notice.

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