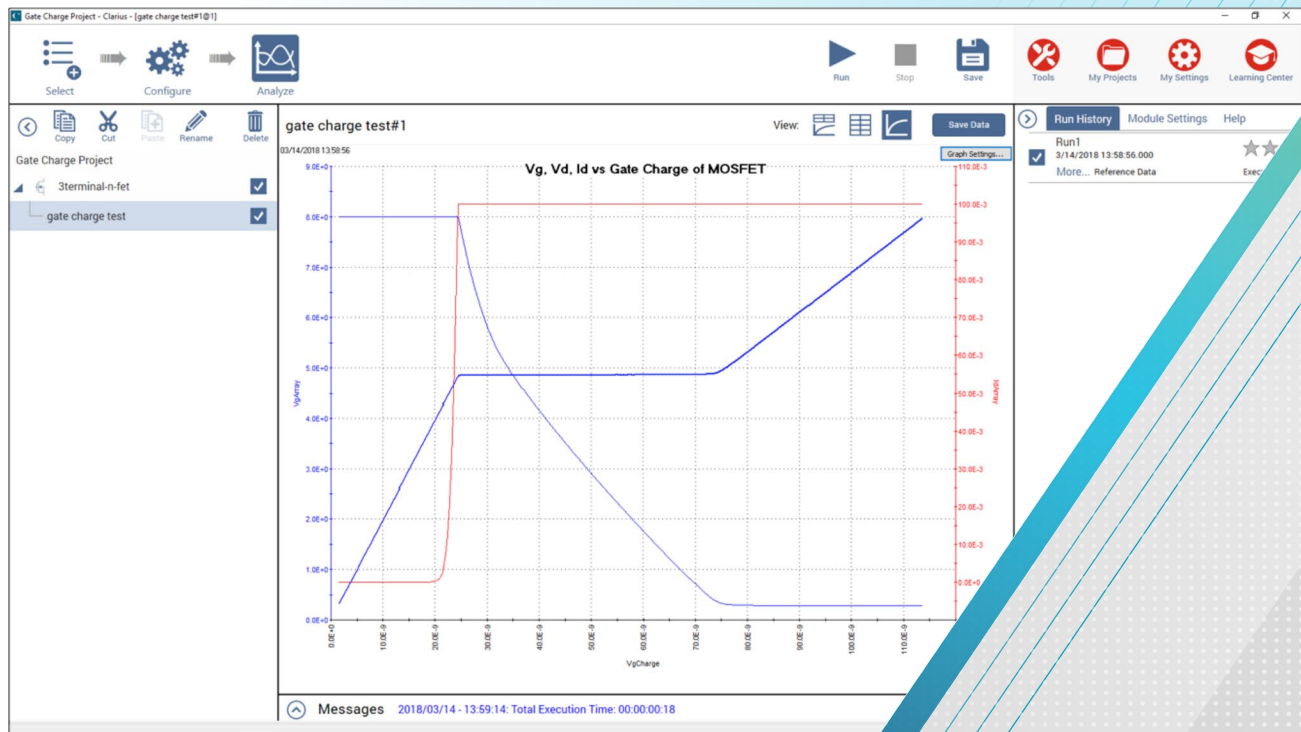


# Measuring MOSFET Gate Charge with the 4200A-SCS Parameter Analyzer

## APPLICATION NOTE



**KEITHLEY**  
A Tektronix Company

**Tektronix**

## Introduction

Power MOSFETs are used in a variety of applications, including as high speed switching devices. The switching speed of the device is affected by internal capacitances and are typically specified in data sheets in terms of  $C_{iss}$  and  $C_{oss}$ , which are derived from the input gate and drain capacitance,  $C_{gs}$  and  $C_{gd}$ . In addition to specifying the capacitance, the gate charge ( $Q_{gs}$  and  $Q_{gd}$ ) can also be used to assess the switching performance of the MOSFET.

One method of measuring the gate charge of a MOSFET is described in the JEDEC JESD24-2 standard, "Gate Charge Test Method". In this method, a gate current is forced while the gate to source voltage is measured as a function of time. From the resulting gate voltage waveform, the gate-source charge ( $Q_{gs}$ ), gate-drain charge ( $Q_{gd}$ ), and gate charge ( $Q_g$ ) are derived.

The 4200A-SCS Parameter Analyzer supports making gate charge measurements on MOSFETs using two source measure unit (SMU) instruments and the gate charge measurement test that's included on the system. This test is one of many included in the extensive Test Library provided in the 4200A-SCS Clarius+ Software Suite. This application note describes how to measure gate charge on a MOSFET based on the JEDEC Gate Charge Test Method using the 4200A-SCS Parameter Analyzer.

## Gate Charge Measurement Overview

In the Gate Charge Method, a fixed test current ( $I_g$ ) is forced into the gate of a MOS transistor and the measured gate source voltage ( $V_{gs}$ ) is plotted against the charge flowing into the gate. A fixed voltage bias is applied to the drain terminal. **Figure 1** shows the gate voltage vs. gate charge of a power MOSFET.

The gate charge ( $Q$ ) is derived from the forced gate current and time, ( $I_g dt$ ). The gate-source charge ( $Q_{gs}$ ) is the charge required, as shown in **Figure 1**, to reach the beginning of the plateau region where the voltage ( $V_{gs}$ ) is almost constant. The plateau (or Miller) voltage ( $V_{pl}$ ) is defined, according to the JEDEC standard, as the gate-source voltage when  $dV_{gs}/dt$  is at a minimum. The voltage plateau is the region when the transistor is switching from the OFF state to the ON state. The gate charge required to complete this switching, that is

the charge needed to switch the device from the beginning of the plateau region to the end, is defined as gate-drain charge ( $Q_{gd}$ ) and is known as the Miller charge. The gate charge ( $Q_g$ ) is the charge from the origin to the point where the gate-source voltage ( $V_{gs}$ ) is equal to a specified maximum ( $V_{gsMax}$ ).

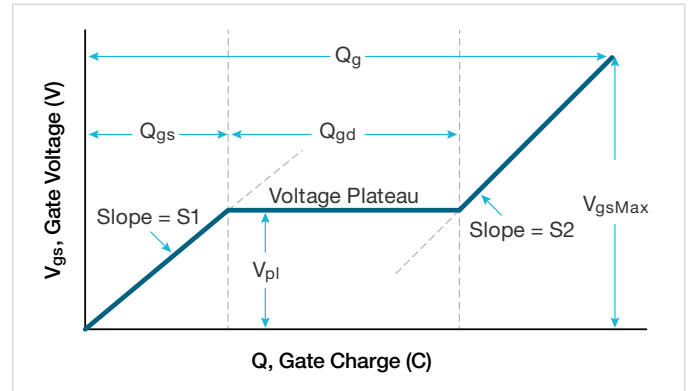


Figure 1. Typical gate voltage vs. gate charge of power MOSFET.

$S1$  is the slope of the line segment from the origin to the first plateau point.  $S2$  is the slope of the line segment from the last plateau point to the specified maximum gate voltage ( $V_{gsMax}$ ). The slopes are used to calculate  $Q_{gs}$  and  $Q_{gd}$ , as specified in the JESD24-2 standard.

**Figure 2** shows typical gate and drain waveforms as a function of time. As current is forced to the gate,  $V_{gs}$  increases until it reaches the threshold voltage. At this point, the drain current ( $I_d$ ) begins to flow. When  $C_{gs}$  is charged up at time  $t1$ ,  $I_d$  stays constant and the drain voltage ( $V_d$ ) decreases.  $V_{gs}$  remains constant until it reaches the end of the plateau. Once  $C_{gd}$  is charged at time  $t2$ , the gate-source voltage ( $V_{gs}$ ) starts to increase again until it reaches the specified maximum gate voltage ( $V_{gsMax}$ ).

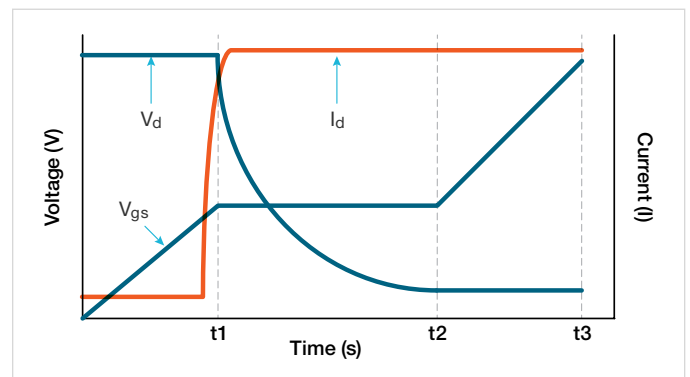


Figure 2.  $V_{gs}$ ,  $V_d$ , and  $I_d$  vs. time of MOSFET.

## Using the 4200A-SCS for Gate Charge Measurements

The 4200A-SCS measures gate charge of a power MOSFET using two SMU instruments. **Figure 3** illustrates the basic circuit diagram of the gate charge test. The Force HI terminal of one SMU (SMU1) is connected to the gate terminal of the MOSFET and forces the gate current ( $I_g$ ) and measures the gate-source voltage ( $V_{gs}$ ) as a function of time. A second SMU (SMU2) applies a fixed voltage ( $V_{ds}$ ) to the drain at a specified current compliance ( $I_{ds}$ ). The maximum compliance current of the 4200-SMU is 0.1 A; the maximum compliance of the 4210-SMU is 1 A.

During the gate charge test, the gate voltage increases and turns ON the transistor. During this transition in the plateau region, the drain SMU (SMU2) switches from voltage control to the current control mode, because the current exceeds the specified compliance level. The software returns the drain current transients and drain voltage during the transition from the OFF state to the ON state.

The MOSFET's source terminal is connected to the Force LO terminal or GNDU of the 4200A-SCS chassis.

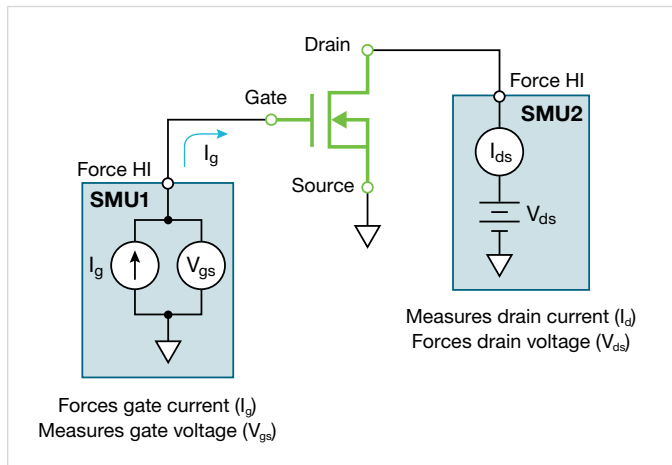


Figure 3. Gate charge test configuration using two SMU instruments.

## Configuring the Clarius+ Software for Gate Charge Measurements

The *Gate Charge* test is located in both the Test and Project Libraries, which can be found from the Select pane by searching for the phrase “gate charge”. Once the test is found

in the Test Library, it can be added to a project by selecting and adding it to the project tree. This test was created from the *gate\_charge* user module in the *GateCharge* user library.

### Input Parameters

Before test execution, the input test parameters are entered in the Configure pane of the Clarius Software (**Figure 4**).

The input parameters will vary depending on the device and which model of SMU is used.

Descriptions of the input parameters are listed in **Table 1**.

First, enter the SMU numbers that are connected to the gate (gateSMU) and drain (drainSMU) of the MOSFET. The source terminal should always be connected to the GNDU, or Force LO.

The magnitude of the current forced to the gate by the gateSMU, is the gateCurrent ( $I_g$ ) parameter. The drain voltage ( $V_{ds}$ ) is the bias voltage applied to the drain and drainLimitI is the compliance current of the drain SMU.

The Coffset parameter is used for correcting for the offset capacitance and is described in the following paragraphs.

Table 1. Input Parameters for *gate\_charge* user module.

Input Parameter	Range of Values	Default Values	Description
gateSMU	SMU1-SMU9	SMU1	The SMU number connected to the gate terminal
drainSMU	SMU1-SMU9	SMU2	The SMU number connected to the drain terminal
source	GNDU	GNDU	The source terminal is always connected to the Force LO terminal on GNDU
Vds	$\pm 200$ V	10 V	The magnitude of the drain bias voltage of the drain SMU
drainLimitI	4200-SMU: 0.1A 4210-SMU: 1 A	0.1 A	Current compliance of the drain SMU
gateCurrent	$\pm 1E-5$ A	1e-7 A	The magnitude of the gate current of the gate SMU
VgsMax	$\pm 200$ V	10 V	The maximum voltage level of the gate SMU.
timeOut	0 to 300 s	60 s	The number of seconds prior to a time out.
measDrain	1 (yes) or 0 (no)	1	Return measured drain current
Coffset	0 or Ceff	0	Run test with open circuit and then enter Ceff value returned to the Sheet

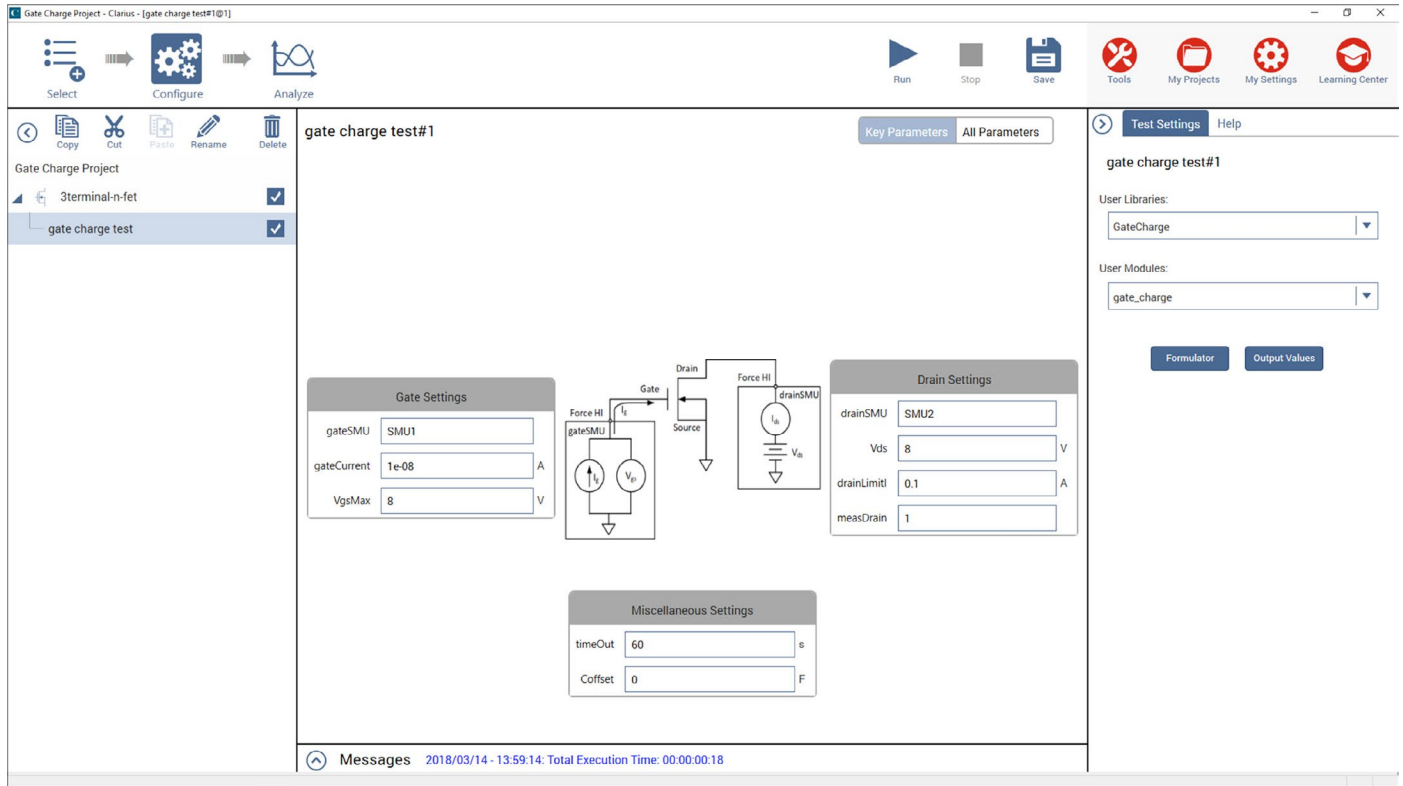


Figure 4. The *gate charge* test in the Configure View.

## Correcting for Offset Capacitances

Depending on the cabling and connections of the measurement system, the offset capacitance can be in the single picofarads to hundreds of picofarads ranges. These capacitances can be corrected by executing the *gate\_charge* user module with an open circuit, obtaining the offset capacitance, then entering in the offset capacitance value in the software for compensation. Here's how these steps are performed:

1. **Measure the offset capacitance.** Set up the test parameters including the input gate current as though the device were connected to the SMUs. However, increase the  $V_{gsMax}$  just for the  $C_{eff}$  measurement. Prior to executing the test, lift the probes or remove the device from the test fixture. Execute the *Gate Charge* test with an open circuit.
2. **Obtain the offset capacitance.** After the test is executed, the measured offset capacitance of the system is calculated and appears in the  $C_{eff}$  column in the Sheet.  $C_{eff}$  is derived from the maximum gate voltage, gate current, and time.
 

Because an open circuit is measured during this step, a Test Status Value of  $-9$  or  $-12$  may appear in the Sheet after the test is executed. This is because no device is measured so there is no plateau region. However, the  $C_{eff}$  value is correct and can be entered as the  $C_{offset}$  in the Configure view.
3. **Enter the measured offset capacitance and execute.** Enter the measured offset capacitance,  $C_{eff}$ , for  $C_{offset}$  in the Configure view. By default,  $C_{offset}$  is 0 F. Compensation will be made for the offset capacitance in subsequent readings.

### Executing the Test

Once the input parameters have been entered, execute the test by selecting Run at the top of the screen. As the test is running, the gate charge waveform will update in real time in the graph in the Analyze view and the calculated output parameters will appear in the Sheet.

### Output Parameters

After the test is completed, several parameters are returned to the Sheet. **Table 2** lists descriptions of these parameters.

Table 2. Output parameters for *gate\_charge* user module.

Output Parameter	Description
gate_charge	Test status values – see Table 3 for descriptions
timeArray	Measured time (seconds)
VgArray	Measured gate-source voltage (volts)
VgCharge	Measured gate charge (coulombs)
VdArray	Measured drain voltage (volts)
IdArray	Measured drain current (amps)
Slope	Dynamic slope (dVg/dt) of gate voltage
Ceff	Ratio of gate charge to maximum gate voltage
Vpl	Plateau or Miller voltage (volts)
T1	Timestamp where the plateau area begins (seconds)
T2	Timestamp where the plateau area ends (seconds)
Qgs	Gate charge from the origin to the first inflection point, or the voltage plateau (coulombs)
Qgd	Gate charge between the two inflection points in the gate charge curve (coulombs)
Qg	Gate charge from the origin to VgsMax (coulombs)

### Graphing the Results

The resulting gate-source voltage can be plotted as a function of the gate charge or the drain current and drain voltage can be plotted as a function of time. **Figure 5** is a typical gate voltage waveform generated by the 4200A-SCS.

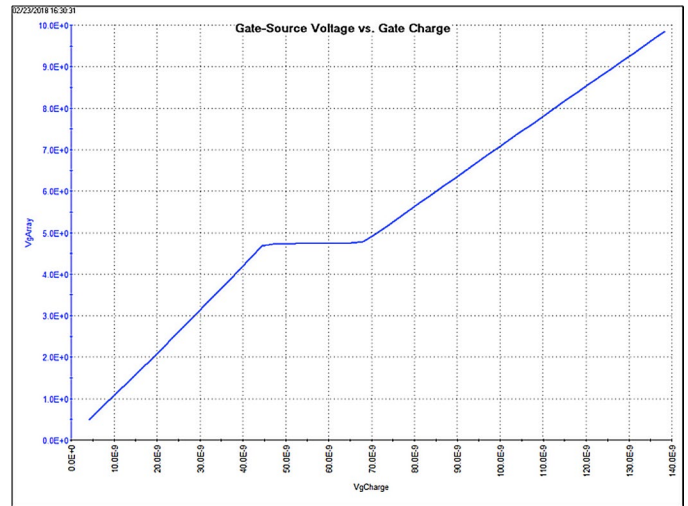


Figure 5. Typical gate voltage waveform generated by the 4200A-SCS.

In addition to plotting  $V_{gs}$ ,  $V_{ds}$ , and  $I_d$  can also be plotted as a function of the gate charge or time. **Figure 6** shows the graph in the Analyze view of the Clarius Software showing all three parameters plotted as a function of the gate charge. In this case, the voltage is shown on the Y1 axis and the current is plotted on the Y2 axis.

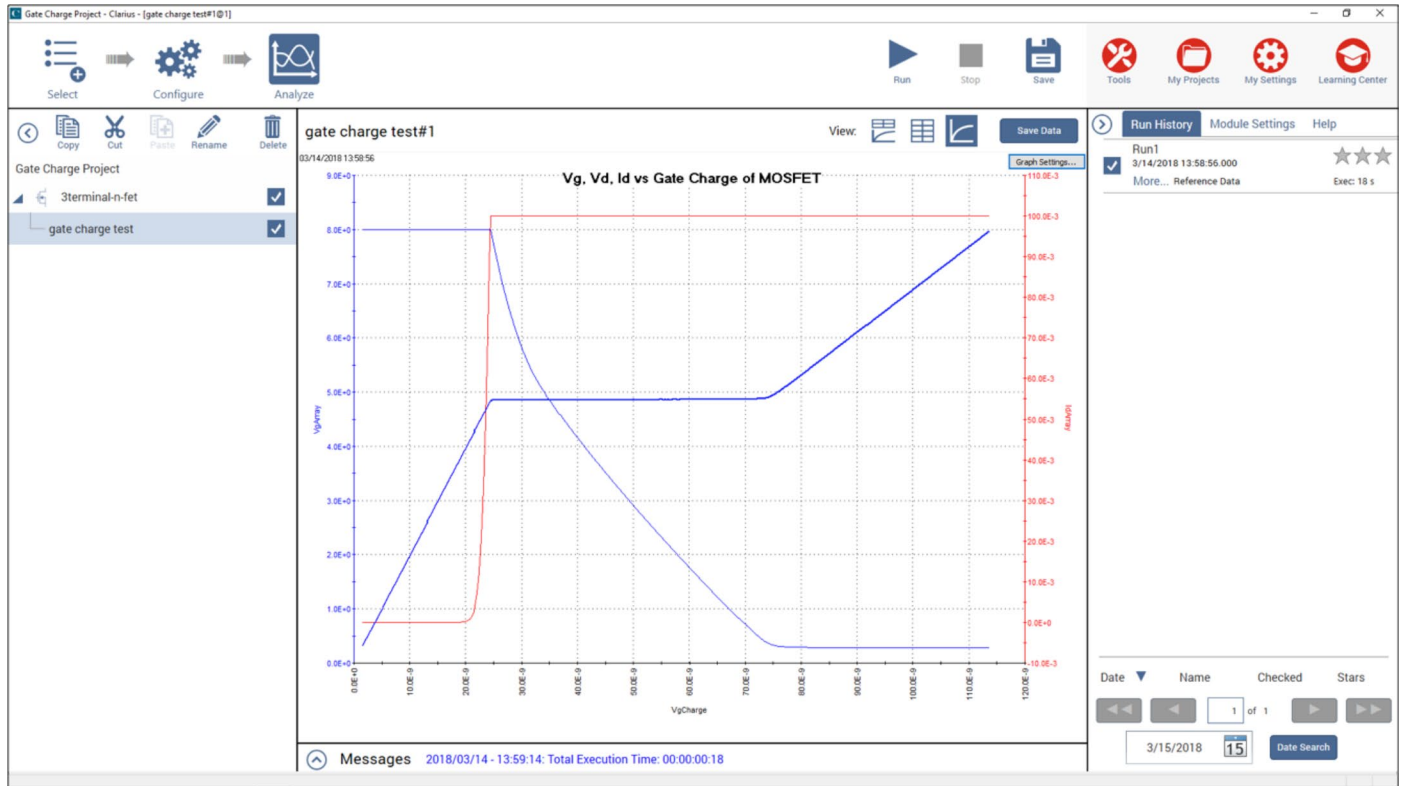


Figure 6.  $V_{gs}$ ,  $V_{ds}$ , and  $I_d$  as a function of gate charge.

### Checking the Test Status

Each time the test is executed, a Test Status Value is returned to the first column in the Sheet, named “gate\_ charge”. **Table 3** lists the returned Test Status Values in the “gate\_charge” column and their corresponding descriptions and notes.

### Conclusion

Gate charge measurements on transistors can be easily made using the 4200A-SCS Parameter Analyzer. Using two SMU instruments connected to the gate and drain of the device, the Clarius Software easily derives the gate charge waveforms.

Table 3. Test Status Values

Test Status	Description	Notes
1	No errors	Test successful.
-1	Gate SMU is not present	Specify correct SMU.
-2	Drain SMU is not present	Specify correct SMU.
-3	VgsMax > 200 V	Verifies gate voltage is less than 200V. Reduce gate voltage.
-4	Drain current limit exceeds 1 A (4210-SMU) Drain current limits exceeds 0.1 A (4200-SMU)	Verifies drain current is less than 1 A (or 0.1A for medium power SMU). Reduce drain current limit (drainLimitI).
-5	Power limit exceeded	Current should be < 0.1A if V >20V. Decrease drain current limit (drainLimitI) or drain voltage (Vds).
-6	Error check on input conditions. Limits timeOut to 200 s.	Specify timeOut to <200 s.
-7	Test time exceeds specified time out (timeOut).	Increase timeOut. Maximum is 200 s. Try increasing gateCurrent to charge up device faster.
-8	Number of iterations/measurements >10000.	Increase gate current (gateCurrent).
-9	Number of iterations/measurements <5	Decrease gate current (gateCurrent). Check device, test set-up and for correct SMU. This error can be ignored if it occurs while measuring an open circuit for offset correction. The Ceff value is still valid.
-10	Number of points from origin to first plateau point is <10	Decrease gate current (gateCurrent)
-11	Error calculating slope, S1. Correlation factor < 0.9. Curve from origin to first plateau point is not linear.	Check device and test set-up.
-12	Error calculating slope, S2. Correlation factor <0.9. Curve from last plateau point to VgsMax is not linear.	Check device and test set-up. If VgCharge or VdArray appear high, try reducing gateCurrent and repeat test. This error can be ignored if it occurs while measuring an open circuit for offset correction. The Ceff value is still valid.
-13	Vds > 200 V	Decrease drain voltage.
-14	gateCurrent > 10 $\mu$ A	Decrease gate current (I <sub>g</sub> ).

## Contact Information

**Australia\*** 1 800 709 465  
**Austria** 00800 2255 4835  
**Balkans, Israel, South Africa and other ISE Countries** +41 52 675 3777  
**Belgium\*** 00800 2255 4835  
**Brazil** +55 (11) 3759 7627  
**Canada** 1 800 833 9200  
**Central East Europe / Baltics** +41 52 675 3777  
**Central Europe / Greece** +41 52 675 3777  
**Denmark** +45 80 88 1401  
**Finland** +41 52 675 3777  
**France\*** 00800 2255 4835  
**Germany\*** 00800 2255 4835  
**Hong Kong** 400 820 5835  
**India** 000 800 650 1835  
**Indonesia** 007 803 601 5249  
**Italy** 00800 2255 4835  
**Japan** 81 (3) 6714 3086  
**Luxembourg** +41 52 675 3777  
**Malaysia** 1 800 22 55835  
**Mexico, Central/South America and Caribbean** 52 (55) 56 04 50 90  
**Middle East, Asia, and North Africa** +41 52 675 3777  
**The Netherlands\*** 00800 2255 4835  
**New Zealand** 0800 800 238  
**Norway** 800 16098  
**People's Republic of China** 400 820 5835  
**Philippines** 1 800 1601 0077  
**Poland** +41 52 675 3777  
**Portugal** 80 08 12370  
**Republic of Korea** +82 2 6917 5000  
**Russia / CIS** +7 (495) 6647564  
**Singapore** 800 6011 473  
**South Africa** +41 52 675 3777  
**Spain\*** 00800 2255 4835  
**Sweden\*** 00800 2255 4835  
**Switzerland\*** 00800 2255 4835  
**Taiwan** 886 (2) 2656 6688  
**Thailand** 1 800 011 931  
**United Kingdom / Ireland\*** 00800 2255 4835  
**USA** 1 800 833 9200  
**Vietnam** 12060128

\* European toll-free number.

If not accessible, call: +41 52 675 3777

Rev. 090617



Find more valuable resources at [TEK.COM](http://TEK.COM)

Copyright © Tektronix. All rights reserved. Tektronix products are covered by U.S. and foreign patents, issued and pending. Information in this publication supersedes that in all previously published material. Specification and price change privileges reserved. TEKTRONIX and TEK are registered trademarks of Tektronix, Inc. All other trade names referenced are the service marks, trademarks or registered trademarks of their respective companies.

042518.SBG 1KW-61388-0

