

# HIGH SPEED INTERFACE STANDARDS

PCI Express | DDR4 | USB | SAS/SATA

eGuide



Next generation interface standards are pushing the limits of today's compliance and debug tools. Electrical validation of PCIe 4.0 16 Gb/s, SAS 12 Gb/s, SuperSpeed USB 10Gb/s, and DDR4 3200 MT/s and other high-speed bus technologies require even more complex test considerations than before. Transmitter performance, for example, is best evaluated with new analysis techniques that can accurately identify jitter & noise from sources such as crosstalk or other multi-lane noise coupling. With a closed eye architecture, commonly found in long channel designs, physical layer testing requires advanced techniques such as channel de-embedding and end-to-end link simulation with reference receivers.



Tektronix automation software simplifies the complexities of validating next-generation high-speed interfaces.

### Design Challenges



- Smaller device geometries coupled with multi-layer PCBs incorporating buried via limit signal access
- Bus behavior with new power-saving schemes including frequency switching and clock gating
- Initiating test mode in-band through the channel, i.e., talk to the receiver's link training and status state machine
- Validating new signal encoding and equalization capability found in high-speed signaling interfaces
- Increasing complexity and quantity for electrical validation – so many tests, so little time!

### Standards

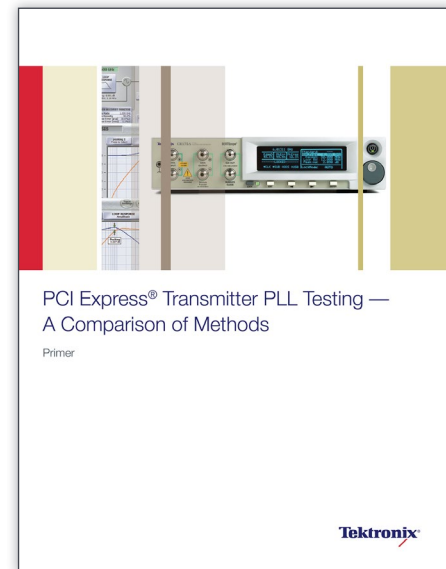


- a. PCI Express
- b. DDR4
- c. USB
- d. SAS/SATA

PCI Express is a high-speed serial computer expansion bus standard designed to replace the older PCI, PCI-X, and AGP bus standards. PCIe has a variety of improvements over the older standards, including higher maximum system bus throughput, lower pin count and smaller physical footprint. PCI Express recently released its 3rd generation specification to operate @ 8 Gb/s and work is underway to define the 4th generation specification targeted to operate @ 16 Gb/s.

[PCISIG.com](http://PCISIG.com)

Get our Primer on PCI Express® Transmitter PLL Testing – A Comparison of Methods



### Design Challenges



- Validating all bus speeds and presets per lane, for example, 8 Gb/s requires testing at 5 Gb/s and 2.5Gb/s with 11 de-emphasis presets on up to 16 lanes
- Placing the device into loopback to perform stressed receiver eye measurements
- Tracking link training sequences to validate speed and link width negotiation between transmitter and receiver

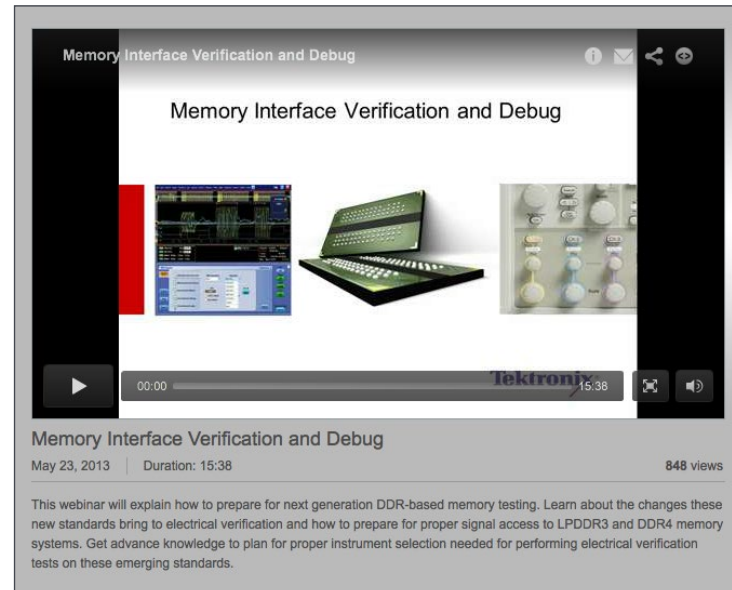
### Tektronix Solution



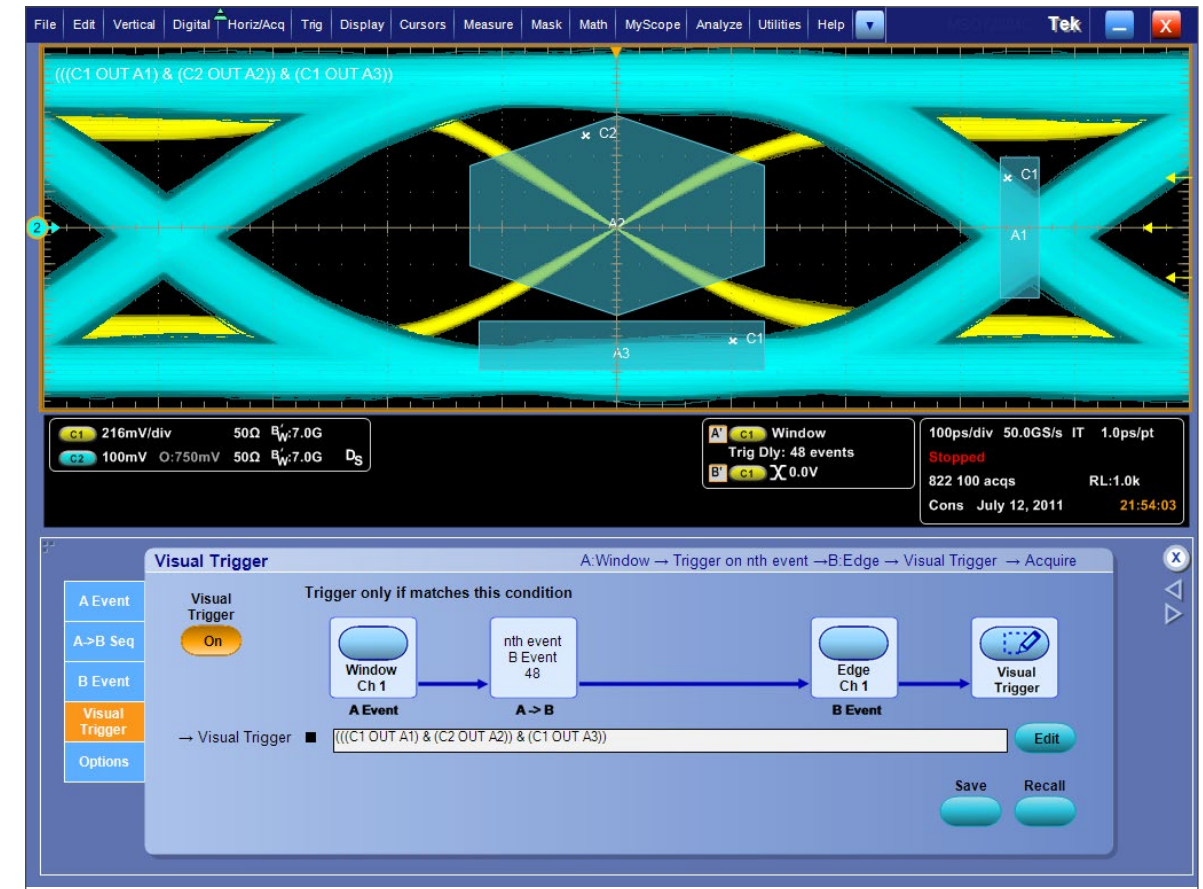
- TekExpress for PCI Express automation software for in-depth compliance testing
- DPO70000SX Series Oscilloscope provides support for 8 and 16 Gb/s debug and validation
- DPOJET and SDLA advanced link analysis for host and device system modeling
- BERTScope PCIe automation simplifies calibration and receiver tolerance testing
- TLA Logic Protocol Analyzer to trace and validate link layer behavior

DDR4 is the next generation memory standard targeted for enterprise computing. The standard enables higher capacity DIMM's (128 GB), doubles the data rate (3200 MT/s) and operates at lower voltage (1.2V) compared to the previous generation.

[JEDEC.org](http://JEDEC.org)



Watch our Webinar on Memory Interface Verification and Debug



Tektronix Visual Trigger can accurately capture fast reads & writes on DDR signaling

### Design Challenges



- Signal Access for debug and validation
- Read / Write separation for analysis
- De-embedding to remove the effects of the interposer and probe, and to view signals @ the memory controller
- Triggering on error conditions such as data-dependent errors
- Protocol error checking

### Tektronix Solution

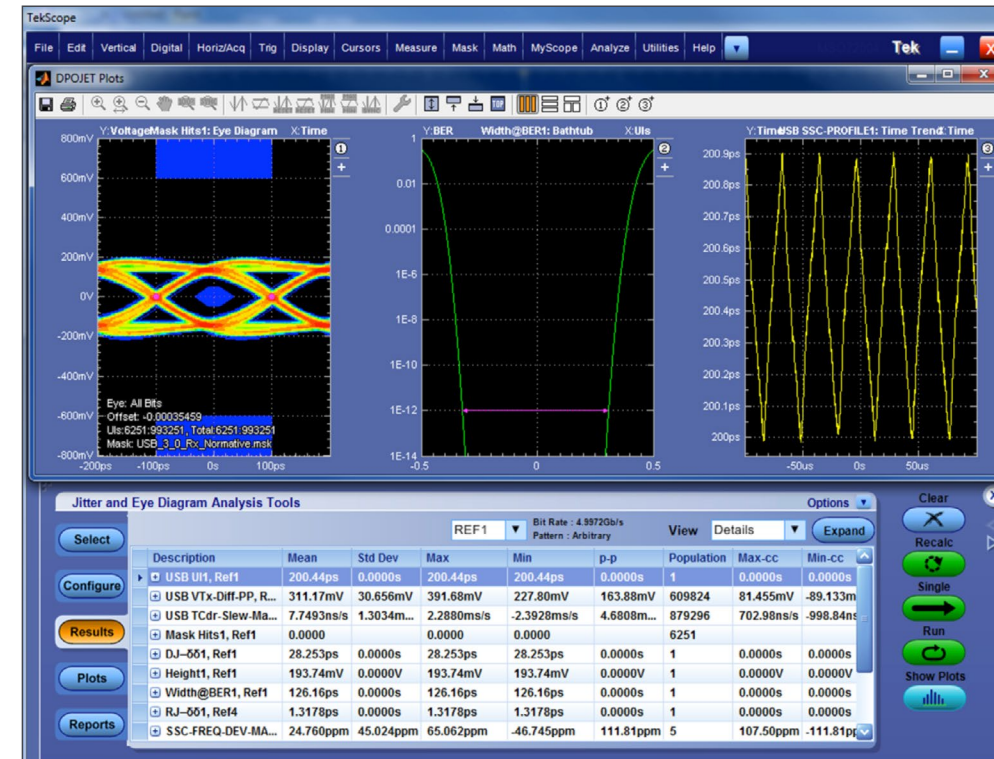
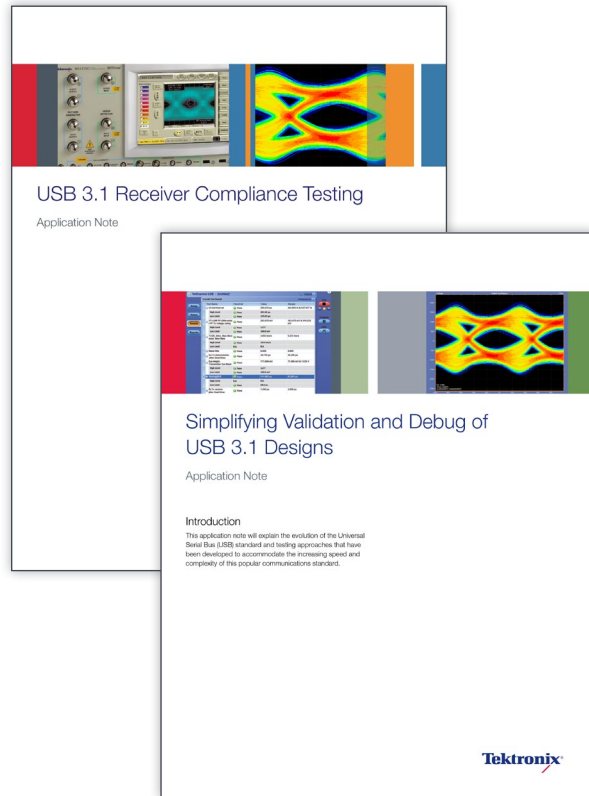


- P7700 Series Probing System with lightweight, flexible interconnected tips
- Interposer solutions enable signal access for both electrical and protocol validation
- DDRA automatically separates Reads / Writes then performs the relevant measurements
- Visual Trigger can be used to define complex conditions, enables capturing conditions of interest
- The TLA7000 Logic Analyzer and the MCA5000 Memory compliance analyzers can be used to perform Logic validation and protocol compliance

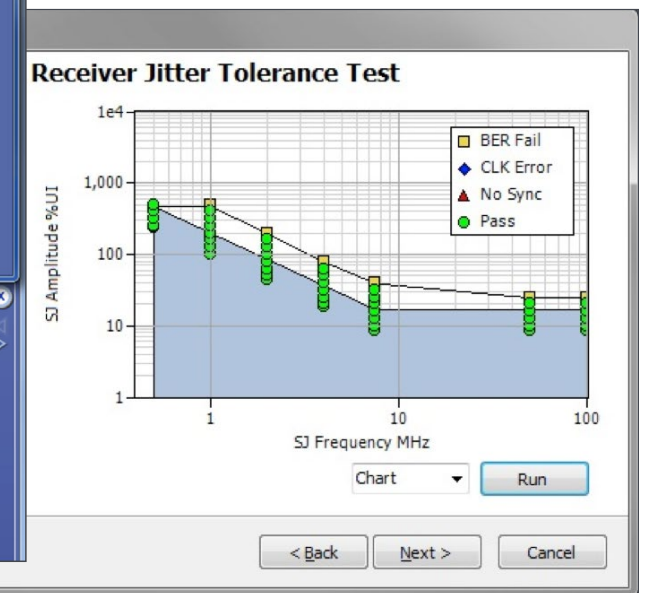
USB 3.1 extends the performance range of USB up to 1GB/s by doubling the SuperSpeed USB clock rate to 10Gbps and enhancing data encoding efficiency. Additionally, the new USB Type-C connector greatly improves the user experience through high power, high bandwidth and a flexible mechanical design.

[USB.org](http://USB.org)

**Get your FREE application kit for USB 3.1 Transmitter and Receiver Testing**



Quickly perform USB 3.1 transmitter eye, jitter, and timing measurements using Tektronix' automated USB 3.1 analysis software.



Characterize your USB 3.1 receiver performance with built-in jitter tolerance margin testing with the BSAUSB31 testing software.

### Design Challenges

- Higher data rate means lower margins
- Long-channel signal recovery requires complex equalization
- 128b/132b encoding requires new LTSSM
- Backwards compatibility means more tests

### Tektronix Solution

- DPOJET and SDLA: Advanced jitter and link analysis for host and device system modeling
- BERTScope USB 3.1 automation simplifies calibration and receiver tolerance testing
- TekExpress USB 3.1 Transmitter test software with comprehensive support for 5/10 Gb/s
- DPO7000SX Series Oscilloscope provides signal integrity for USB 3.1 margin analysis

Next-generation storage technologies such as 12 Gb/s SAS and SATA enable a new performance class of storage hierarchy that unlocks the performance of servers and solid-state drives.

[t10.org](http://t10.org)

[scsita.org](http://scsita.org)

[sata-io.org](http://sata-io.org)

### Methods of Implementation

- SAS MOI
- SATA MOI

The screenshot displays the TekExpress SAS software interface. On the left, a navigation pane shows steps: Setup, DUT, Test Selection (highlighted), Acquisitions, and Preferences. The main area shows a tree view of test categories: OOB (5.1.1-5.1.4), PHY (5.2.1-5.2.5), and TSG (5.3.1-5.3.4). A 'Test Description' box provides details for the selected OOB test. On the right, a 'TX Common Mode Voltage Spectral Measurement' window shows a spectral plot with a yellow signal band between -50 and 0 dBmV across a 50 GHz frequency range. Below this, a 'Jitter and Eye Diagram Analysis Tools' window shows an 'Overall Test Result: Pass' and a table of test results.

Description	Pass/Fail	Mean	Std Dev	Max	Min	p-p	Population
CM RMS1, Math1	Pass	21.114m	0.0000	21.114m	21.114m	0.0000	1
CM Spectrm 2nd Hr...	Pass	4.9486	0.0000	4.9486	4.9486	0.0000	1
CM Spectrm Fndl Fre...	Pass	14.076	0.0000	14.076	14.076	0.0000	1

Simplify complex physical layer measurements with the TekExpress for SATA/SAS transmitter test software.

Perform timing, jitter and amplitude analysis with DPOJET software

### Design Challenges



- Complex bus topology and routing requires advanced equalization such as FFE/DFE.
- New host architectures include extensive Tx emphasis capabilities which can cause interoperability issues
- Independent clock domains require inclusion of logical idle characters between a transmitter and receiver



### Tektronix Solution

- DPO70000SX Series Oscilloscope provides 50 GHz bandwidth to capture SAS 22.5 Gb/s
- DPOJET and SDLA advanced link analysis for host and device system modeling
- BERTScope jitter tolerance search mode simplifies receiver margin testing while filtering align primitives
- **TekExpress SATA/SAS Transmitter test software** with comprehensive support for Tx equalization characterization

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